Point-by-point replies to the comments of Referee #1

To esteemed anonymous referee #1.

Your comments impress us a lot. We really appreciate your time and energy for reviewing our manuscript. It is hard for us to express our grateful feeling. In fact, we have learned many things during this revision process, and such experience would be very helpful for our future study. We herewith provide our response to your comments as below:

1. Line54: Please elaborate on what is hysteresis comparator.

Our response:

In order to achieve frequency measurement, we use hysteresis comparison circuit where LM311 plays an important part. LM311 is a low-speed operational amplifier which is exclusively used in voltage comparison, the typical response time is 200ns. We can use a single supply voltage or a dual power supply.

The calculation formula for high hysteresis comparison voltage is as follows:

$$V_{inH} = \frac{R4}{R4 + R2} (V_{OH} - V_{ref}) + V_{ref}$$
 (1)

The calculation formula for low hysteresis comparison voltage is as follows:

$$V_{inL} = \frac{R4}{R4 + R2} (V_{OL} - V_{ref}) + V_{ref}$$
 (2)

And we have already added the above part to our manuscript.

2. Line61: Please explain how you implement the optocoupler isolation.

Our response:

HCPL0723 is a high-speed, positive logic CMOS optocoupler of AVAGO TECHNOLOGIES company, which supports up to 50M bit rate transmission speed, the maximum transmission delay is 22ns, and the external circuit connection is simple, which only needs to add a Coupling capacitors at both ends of the power supply, as shown in Fig. 3. The input and output direction of optocoupler should be confirmed one by one to ensure the correctness of the circuit. Other from traditional optocouplers, the photodiode control pin of HCPL0723 does not flow current, and the output logic pins do not need to be pulled up. Actually, the current that drives the photodiode flows from the input pin (1 pin).

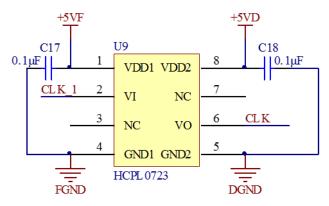


Figure 3: Schematic circuit diagram of high-speed optocoupler isolation

And we have already added the above part to our manuscript.

3. Line91: According to your discussion, the atomic clock is a very important part in your device, so in order to help the author better understand the principles of your instrument, it is necessary to elaborate on its circuit structure.

Our response:

Thanks for your suggestion, we have added the circuit structure of high precision atomic clock to our manuscript.

The block diagram of the high-precision atomic clock circuit is shown in Figure 5. Clock board consists of three parts: MSP430 microcontroller, GPS module and atomic clock module. In addition, the clock board also includes some necessary download ports, configration interface and the interface with the main control board.

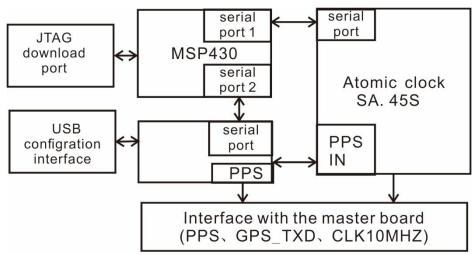


Figure 5: Block diagram of high precision atomic clock circuit

MSP430 microcontroller, the master, downloads the program through the JTAG download port. The microcontroller communicates with the atomic clock SA.45S through serial port 1, receives the serial data to obtain the atomic clock running status, and sends the serial port command to control its taming time. MSP430 and GPS module communicate with each other through serial port 2.

The transmitter of the GPS serial port is also connected to the IO of the FPGA so that the acquisition data contains the location coordinate information. The GPS second pulse signal is connected to the atomic clock of the PPS_IN pin to tame the atomic clock module. GPS sets the mode of operation through its full-speed USB interface, after setting the work mode of host computer software, you can store the work mode information in the internal of GPS, so that host computer can automatically read the last saved work mode information from the internal of GPS when the module power was cut off.